TITLE OF THE INVENTION

DATA MODULATION METHOD AND APPARATUS CAPABLE OF SUPPRESSING DC COMPONENT USING PARITY INFORMATION OF SYNCHRONIZATION CODEWORD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority of Korean Patent Application No. 2003-15856, filed on March 13, 2003, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to data modulation, and more particularly, to a data modulation method capable of suppressing a DC component using parity information of a synchronization codeword, and an apparatus for executing the method.

2. Description of the Related Art

[0003] A multimode coding method is a method of granting DC suppression ability to a modulation code without DC suppression ability. Even though a-bit additional information is inserted in an input data row, 2^a different random data rows are generated, and modulation without DC suppression ability is performed for the 2^a different random data rows, the multimode coding method has DC suppression ability by selecting the modulated data row having the smallest DC component among the 2^a different random data rows.

[0004] In a conventional multiplexing method of converting an input data row into 2^a different random data rows by using the a-bit additional information, input data is transmitted as a run length limited (RLL) stream by consecutively scrambling the input data. However,

if an error is generated in the transmitted RLL stream when inverse data conversion is performed, the error propagates, affecting not only the data where the error was generated but subsequent data as well. Such error propagation is characteristic of a multimode coding method using scrambling.

[0005] Further, in the conventional art, in a case where additional bits for a synchronization codeword and a multiplexing ID are inserted in a data row multiplexed and randomized through consecutive scrambling, or where the multiplexing ID is inserted in the data row according to a size of a data block, regardless of the synchronization codeword, a number of additional bits corresponding to the multiplexing ID increases.

SUMMARY OF THE INVENTION

[0006] The present invention provides a data modulation method capable of effectively suppressing DC components included in modulated codeword streams without reducing a code rate, and an apparatus that executes the method.

[0007] The present invention further provides a data modulation method capable of improving DC component suppression ability by having a bit capable of controlling parity in a synchronization codeword and multiplexing input data according to the parity of the synchronization codeword, and an apparatus that executes the method.

[0008] The present invention further provides a data modulation method capable of effectively suppressing DC components included in modulated codeword streams by including a multiplexing ID in a synchronization codeword, having parity in the multiplexing ID, and controlling parity of a whole synchronization codeword, and an apparatus that executes the method.

[0009] According to an aspect, a data modulation method is provided including: multiplexing input data according to multiplexing information; inserting a synchronization codeword including multiplexing information for a multiplexed data stream, and performing

data modulation and outputting each modulated data stream; and selecting a modulated data stream having a smallest DC component from among the modulated streams.

[0010] According to another aspect, a data modulation method is provided, which converts m-bit source data into an n-bit codeword ($n \geq m$) where a minimum constraint length is d and a maximum constraint length is k, the data modulation method including: multiplexing input data segmented by a predetermined length according to multiplexing information by discontinuously scrambling the segmented input data; inserting a synchronization codeword including the multiplexing information for a multiplexed data stream, and performing run length limited (RLL) modulation and outputting each modulated data stream; and selecting a respective modulated data stream having a DC component, which is smallest from among the modulated data streams.

[0011] According to another aspect, a data modulation apparatus including: a multiplexer, which multiplexes input data according to multiplexing information; a modulator, which inserts a synchronization codeword including the multiplexing information for a multiplexed data stream, and performs modulation and outputs each modulated stream; and a selector, which selects a respective modulated data stream having a DC component which is smallest from among the modulated streams.

[0012] According to another aspect, a data modulation apparatus is provided, which converts m-bit source data into an n-bit codeword ($n \geq m$) where a minimum constraint length is d and a maximum constraint length is k, the apparatus including: a pseudo scramble multiplexer, which multiplexes input data segmented by a predetermined length according to multiplexing information by discontinuously scrambling the segmented input data; a modulator, which inserts a synchronization codeword including the multiplexing information for a multiplexed data stream, and performs run length limited (RLL) modulation and outputs each modulated data stream; and a selector, which selects a respective modulated data stream having a DC component which is smallest from among the modulated streams.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] These and/or other aspects and advantages of the invention will become apparent and more readily appreciated from the following description of the preferred embodiments, taken in conjunction with the accompanying drawings of which:

[0014] FIG. 1 is a block diagram of a data modulation apparatus according to an embodiment of the present invention;

[0015] FIGS. 2A-2C illustrate examples of synchronization codewords to be used in the present invention;

[0016] FIG. 3 is an example of the synchronization codeword made up of a synchronization body and a multiplexing identification (ID) of FIG. 2A;

[0017] FIG. 4 shows how a pseudo scramble multiplexer of the data modulation apparatus of FIG. 1 which generates an input data stream multiplexed in one of two different operations corresponding to input multiplexing information of 0 or 1; and

[0018] FIG. 5 is a graph illustrating a power spectrum density curve showing a DC suppression performance improvement when data is multiplexed by a synchronization codeword according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0019] Reference will now made in detail to the present preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiment is described below in order to explain the present invention by referring to the figures.

[0020] FIG. 1 is a block diagram of a data modulation apparatus according to an embodiment of the present invention. The data modulation apparatus suppresses a DC component of a modulated codeword stream using a synchronization codeword.

[0021] With reference to FIG. 1, an input data row may be expressed by x = (x_0, x_1,..., x_{l-1}) as in Equation 1, and the input data row is divided by vXu (=k) in a vXu divider 10 as in Equation 2, i.e., the input data row is divided by a v-data row, each piece of a data row having u bytes.

[0022]

$$x = (x_0, x_1, \ldots, x_{k-1}, \ldots, x_{l-1})$$

[0023]

$$B_x = \begin{array}{c} \\ \\ \\ \\ \\ J \end{array} \left\| \begin{array}{c} x_{0,0},\ x_{0,1,.}\ \cdots,\ x_{0,\mu-1} \\ x_{1,0},\ x_{1,1},\ \cdots,\ x_{1,\mu-1} \\ \cdots \\ x_{1,0},\ x_{i,1},\ \cdots,\ x_{i,j},\ \cdots,\ x_{i,\mu-1} \\ \cdots \\ x_{y-1,0},\ x_{y-1,1},\ \cdots,\ x_{y-1,\mu-1} \end{array} \right\| \begin{array}{c} \\ \\ \\ \\ \\ K \end{array} = \begin{array}{c} \\ \\ \\ \\ \\ J \end{array} \left\| \begin{array}{c} \underline{y_0} \\ \underline{y_1} \\ \cdots \\ \underline{y_i} \\ \cdots \\ \underline{y_{y-1}} \end{array} \right\| \begin{array}{c} \\ \\ \\ \\ \\ K \end{array}$$

where $x_{i,j} = x_{ixu+j}$.

[0024] After a pseudo scramble multiplexer 20 multiplexes each of the vXu data rows divided by the vXu divider 10 into 2 data rows by adding 1-bit multiplexing information to each of the divided vXu data rows, the pseudo scramble multiplexer 20 converts the two data rows into two pieces of pseudo random data according to the added 1-bit multiplexing information.

[0025] When a conversion into the pseudo random data is finished, two different multiplexed u-byte data are made from one u-byte data row $\underline{y_i}$ as shown in Equations 3 and 4.

[0026]

$$\underline{C_y} = (\underline{C_0}, \underline{C_1}, \ldots, \underline{C_i}, \ldots, \underline{C_{v-1}})$$

[0027]

$$C_i = \begin{bmatrix} s_0, & y_{i,0}^0, & x_{i,1}, \ldots, & x_{i,q-1}, & y_{i,q}^0, & x_{i,q+1}, \ldots, & y_{i,p*q}^0, \ldots, & x_{i,u-1} \\ s_1, & y_{i,0}^1, & x_{i,1}, \ldots, & x_{i,q-1}, & y_{i,q}^1, & x_{i,q+1}, \ldots, & y_{i,p*q}^1, \ldots, & x_{i,u-1} \end{bmatrix} = \begin{bmatrix} f(\underline{y_i}/s_0) \\ f(\underline{y_i}/s_1) \end{bmatrix}$$

Here, u-1 is a multiple of q, p = 0, 1,..., r, and r = (u-1)/q.

[0028] Function $f(\underline{y_i}/s_0)$ and function $f(\underline{y_i}/s_1)$ are two pieces of random data made from the input data row $\underline{y_i}$ using the1-bit multiplexing information.

[0029] Each of first and second synchronization/multiplexing ID inserters 31 and 32 of a synchronization codeword inserter 30 inserts a synchronous codeword including a multiplexing ID converted from the multiplexing information in each of the two multiplexed pseudo random data rows, i.e., each of the two pseudo random data rows multiplexed by the multiplexing information. The multiplexing ID includes a parity control bit capable of suppressing a DC component included in the multiplexed codeword stream according to whether a parity of the multiplexed codeword stream is even or odd.

[0030] First and second weak DC-free RLL encoders 41 and 42 of an encoder 40 may include two channels according to the added multiplexing information, and may use a RLL modulation method. In particular, the first and second weak DC-free RLL encoders 41 and 42 may utilize a code of a weak DC-free RLL modulation method that does not have an additional DC suppression control code conversion table having an additional bit, so if there is no redundancy, DC suppression is possible but DC suppression performance decreases. The RLL modulation method converts m-bit source data into an n-bit codeword (n≥m) where a minimum constraint length is d and a maximum constraint length is k.

[0031] That is, in a case where the encoder 40 performs weak-DC free RLL modulation without using the DC suppression control conversion table having an additional bit, the encoder 40 generates codewords suited to predetermined constraint length conditions, groups the codewords according to the predetermined constraint length conditions, and performs the RLL modulation using a main code conversion table including the codewords so that a code row of a source word has a DC control ability, and a DC suppression control subconversion table for codewords that satisfy the predetermined constraint length conditions and are not required in the main code conversion table. The synchronization codeword inserter 30 and the encoder 40 may be called a modulator.

[0032] A comparison/selection unit 50 compares RLL-modulated streams from the two channels and selects the modulated stream having a smaller DC component.

[0033] When m denotes a number of bits of data before modulation and n denotes a number of bits of a codeword after modulation, the data is multiplexed using a synchronization codeword such that the DC component included in a modulated codeword stream is more effectively suppressible without decreasing a code rate (i.e., a proportionality of m/n).

[0034] That is, the synchronization codeword comprises a synchronization body, which denotes a synchronous signal, and a multiplexing ID. The multiplexing ID is a parity control ID used to control a number of bits having a value of 1 in the synchronization codeword to be an even number or an odd number. For example, the synchronization codewords may be built as shown in FIGS. 2A-2C. In FIGS. 2A-2C, the synchronization body is a specific pattern belonging only to synchronous signals. For example, the specific pattern may be a pattern with a longest run length that is not included in other codewords. The multiplexing ID in the synchronization codeword makes a total number of bits having a value of 1 within a whole synchronization codeword an odd number or an even number. The multiplexing ID may be attached to or mixed in with the synchronization ID, which is used to classify another characteristic of the synchronization codeword.

[0035] A first type of synchronization codeword includes a synchronization body and a multiplexing ID controlling parity, as shown in FIG. 2A. A type of second synchronization codeword includes a synchronization body, a synchronization ID, and a multiplexing ID controlling the parity, as shown in FIG. 2B. A third type of synchronization codeword includes a synchronization body and a synchronization ID mixed in with a multiplexing ID controlling the parity, as shown in FIG. 2C.

[0036] FIG. 3 is an example of the first type of the synchronization codeword comprising the synchronization body and the multiplexing ID.

[0037] With reference to FIG. 3, in a modulation code where a minimum run length is 1 and a maximum run length is 7, the synchronization body classifies the synchronous signal using a run length of 8, which violates a k condition, and the multiplexing ID includes a parity control bit (displayed as x) to control the parity of the synchronization codeword. Regardless of the type of the synchronization codeword (three different types of synchronization codewords are shown in FIGS. 2A-2C), the parity control bit x operates according to a common principle to make a number of bits having a value of 1 in the synchronization codeword into an even number or an odd number.

[0038] When the multiplexing information multiplexing an input data row is 0, the synchronization ID and the multiplexing ID corresponding to the multiplexing information form the synchronization codeword having an even parity. Conversely, when the multiplexing information multiplexing the input data row is 1, the synchronization ID and multiplexing ID corresponding to the multiplexing information form the synchronization codeword having an odd parity.

[0039] FIG. 4 shows how a pseudo scramble multiplexer 20 of FIG. 1 generates an input data stream multiplexed in one of two different ways corresponding to the input multiplexing information being 0 or 1.

[0040] A pseudo scramble multiplexing method refers to a method of discontinuously scrambling the input data and, otherwise, does not refer to a multiplexing method of

continuously scrambling input data. In the multiplexing method of continuously scrambling the input data, an error occurring at a certain position propagates to subsequent data. However, if data is scrambled in a discontinuous manner within a limit of not affecting a DC component of a code row, a probability of such error propagation is reducible.

[0041] In FIG. 4, $\underline{y_i}$, an input data row having a length of u bytes comprising predetermined bits of data $x_{i,0}|x_{i,u-1}$, is converted into pseudo random data $f(\underline{y_i}/0)$ or $f(\underline{y_i}/1)$ through 1-bit multiplexing information (0 or 1) and exclusive OR (EXOR) operations by EXOR gates disposed every qth term corresponding to a scramble period which is not continuously disposed.

[0042] By performing an EXOR operation on an initial unit of data to be modulated $x_{i,0}$ (called a code modulation unit) and 1-bit initial data (multiplexing information), converted data $y^t_{i,0}$, which corresponds to the initial code modulation unit and does not include the initial data, is generated. Code modulation units $x_{i,1}$ through $x_{i,q-1}$ are output without any EXOR operation, and then the EXOR operation is again performed on the converted data $y^t_{i,0}$ of the initial code modulation unit and a qth code modulation unit $x_{i,q}$ to produce the next converted data $y^t_{i,q}$ in a common manner as that of $y^t_{i,0}$. In this manner, the EXOR operations are repeated every qth unit up to a final code modulation unit of the input data row $\underline{y_i}$.

[0043] FIG. 5 is a graph illustrating a power spectrum density (PSD) curve showing a DC suppression ability when a synchronization codeword is used as the multiplexing information. FIG. 5 shows that DC suppression is improved when the input data is multiplexed according to the parity (i.e., even or odd parity) of the synchronization codeword having a parity bit controlling the parity within the synchronization codeword. When data is multiplexed according to the parity bit of the synchronization codeword with a scramble spacing index q=5, the DC suppression ability (i.e., effect) is 4dB greater than when the data is not multiplexed.

[0044] As described above, a DC component included in a modulated codeword stream is more effectively suppressible without a decrease in a code rate by multiplexing input data

according to a parity (i.e., even or odd parity) of a synchronization codeword having a parity bit controlling the parity within the synchronization codeword.

[0045] Although a few preferred embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes may be made in this embodiment without departing from the principles and spirit of the invention, the scope of which is defined in the claims and their equivalents.